

IN THE CLAIMS:

Claims are presented below in format for publication. Claims 1, 2, 6-9, 11-16, 19, and 20 have been amended. Please enter these claims as amended. Claims 21 through 29 have been withdrawn from consideration as being drawn to a non-elected invention. Attached is Appendix A, which contains a marked-up version of the claims as revised.

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1. (Amended) A chip-scale package comprising:

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a semiconductor die having an active surface having at least one bond pad thereon;
at least one conductive trace having an upper surface and a lower surface, the lower surface of said at least one conductive trace substantially non-conductively attached to a portion of the active surface of said semiconductor die;
at least one conductive bond connecting the at least one conductive trace to the at least one bond pad on the active surface of said semiconductor die;
at least one carrier bond attached to the upper surface of the at least one conductive trace; and
an encapsulant material encapsulating said semiconductor die, the at least one conductive trace, the at least one conductive bond and a portion of the at least one carrier bond, the at least one carrier bond having another portion extending beyond said encapsulant material.

2. (Amended) A chip-scale package comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon;
a dielectric element having an upper surface and a lower surface, the lower surface of said dielectric element attached to a portion of the active surface of said semiconductor die;
a plurality of conductive traces, each trace of the plurality of conductive traces having an upper surface and a lower surface, the lower surface of each trace of said plurality of conductive traces attached to a portion of the upper surface of said dielectric element for connecting each conductive trace of said plurality of conductive traces to the active surface of said semiconductor die;
a plurality of conductive bond members, at least one conductive bond member of the plurality of conductive bond members connecting each conductive trace of said plurality of

conductive traces to at least one bond pad of the plurality of bond pads on the active surface of said semiconductor die;
a plurality of conductive carrier bonds, at least one carrier bond of the plurality of conductive carrier bonds disposed on the upper surface of each conductive trace of said plurality of conductive traces; and
an encapsulating material disposed about at least portions of said semiconductor die, said dielectric element, said plurality of conductive traces, said plurality of conductive bond members and a portion of each carrier bond of said plurality of carrier bonds.

3. A chip-scale package as in claim 2, wherein said dielectric element includes an adhesive-coated polyimide tape.

4. A chip-scale package as in claim 2, wherein said dielectric element includes a polyimide film.

5. A chip-scale package as in claim 2, wherein the upper surface and lower surface of said dielectric element are attached respectively to a portion of the lower surface of each conductive trace of said plurality of conductive traces and a portion of the active surface of said semiconductor die connecting portions of said plurality of conductive traces and portions of said semiconductor die.

6. (Amended) A chip-scale package as in claim 2, wherein said plurality of conductive traces comprises a plurality of lead fingers.

7. (Amended) A chip-scale package as in claim 2, wherein said plurality of conductive traces comprises a conductive metal.

8. (Amended) A chip-scale package as in claim 2, wherein said plurality of conductive bond members comprises a conductive metal.

9. (Amended) A chip-scale package as in claim 2, wherein said plurality of conductive bond members comprises bond wires.

10. A chip-scale package as in claim 9, wherein said bond wires comprise gold or aluminum.

11. (Amended) A chip-scale package as in claim 2, wherein said plurality of conductive bond members comprises TAB bonds.

12. (Amended) A chip-scale package as in claim 2, wherein said plurality of conductive bond members comprises thermocompression bonds.

13. (Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds includes metal.

14. (Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds comprises a conductive or conductor-filled polymer.

15. (Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds is selectively located on the upper surface of said plurality of conductive traces forming an array.

16. (Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds comprises solder balls.

17. A chip-scale package as in claim 2, wherein said encapsulating material comprises a substantially non-conductive material.

18. A chip-scale package as in claim 2, wherein said encapsulating material comprises a material having a low modulus of elasticity.

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19. (Amended) A chip-scale package as in claim 2, wherein each conductive carrier bond of said plurality of conductive carrier bonds further comprises an upper portion and a lower portion, said lower portion of a conductive carrier bond attached to the upper surface of a conductive trace of said plurality of conductive traces.

20. (Amended) A chip-scale package as in claim 19, wherein said encapsulating material is disposed about the lower portions of said plurality of conductive carrier bonds.
